

ABSTRACT OF THE DISCLOSURE

This invention is a process for manufacturing a random access memory array. Each memory cell within the array which results from the process incorporates a stacked capacitor, a silicon nitride coated access transistor gate electrode, and a self-aligned high-aspect-ratio digit line contact having a tungsten plug which extends from the substrate to a metal interconnect structure located at a level above the stacked capacitor. The contact opening is lined with titanium metal which is in contact with the substrate, and with titanium nitride that is in contact with the plug. Both the titanium metal and the titanium nitride are deposited via chemical vapor deposition reactions.

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